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EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/16/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/802,519	ANNAYYA ET AL.	
	Examiner	Art Unit	
	Mujtaba K. Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16 and 20-22* is/are rejected.

7)☒ Claim(s) *17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-22 are presented for examination.

Information Disclosure Statement

The references listed in the information disclosure statements (IDS) submitted March 16, 2004 have been considered. The submission is in compliance with the provisions of 37 CFR 1.97. PTO-1449 is signed and attached.

Oath/Declaration

The Oath filed March 16, 2004 complies with all the requirements set forth in MPEP 602 and therefore is accepted.

Drawings

The drawings submitted March 16, 2004 are objected to because:

- Figure 1A should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

- Figure 1B should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.
- The Examiner would like to point out that there are certain reference numbers in the specification that do not correspond directly with the figures. For example, in figure 2 the reference number 260 refers to the physical interface device and on page 11 of the specification, line 6 the reference number 260 has a subscript 1 after it. Applicants are suggested to make a clear distinction between the two, if any. Otherwise it is strongly recommended to use uniform reference numbers throughout the specification and figures.

Appropriate correction is requested.

Specification

The specification is objected to because:

- There is no "brief summary of invention" section after the "background" as required. See MPEP 608.01(a) [R-5].
- In paragraph 0033, last sentence the semicolon (;) should be replaced with a period (.) and after the semicolon it should begin with "Accordingly".

Correction is requested.

Claim Objections

Claim 2 is objected to because of the following informalities:

- In line 1, the claim recites, "...the nullifier..." and it should recite, "...the CRC nullifier..." to avoid unnecessary confusion. The Examiner will interpret it as such.

Appropriate correction is required.

Claim 17 is objected to because of the following informalities:

- The claim is not terminated with a period. The Examiner will interpret it with a period. See MPEP 608.01(m) [R-3].

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8, 11, 13, 14 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen (USPAN 2003/0093752A1).

As per claim 1, Chen teaches an apparatus (i.e., title and paragraph 0002) comprising: a cycle redundancy check (CRC) calculator (i.e., Figure 3A and paragraph 0033); and a CRC nullifier coupled to the CRC calculator (i.e., Figure 3A, reference numbers 336, 338 and 340 & paragraphs 0011, 0052-0056). The Examiner would like to explain the interpretation of the CRC nullifier. In paragraph 0011 (lines 9-12), Chen teaches to nullify a subset of the shift registers used in the CRC generator. Further in paragraphs 0052-0056, Chen performs the nullification process by programmable registers Y which are shown in Figure 3A and referred to by reference numbers 336, 338 and 340. Particularly, in paragraph 0055 (lines 5-9) Chen explains the nullifier by determining which of the coefficients take the value of 0.

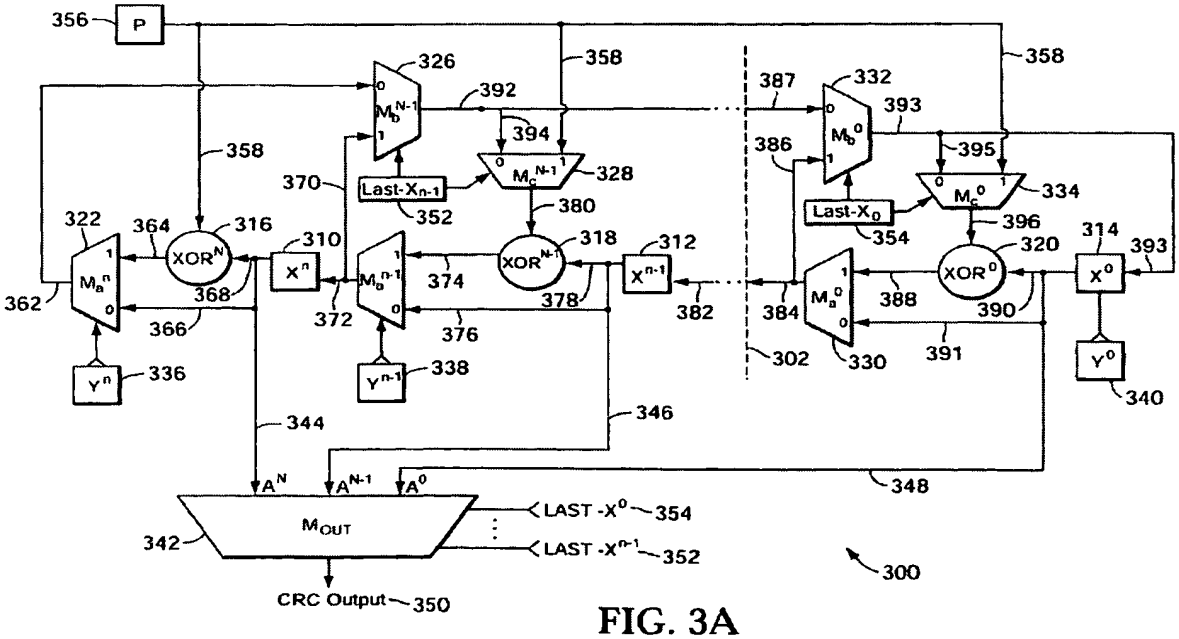


FIG. 3A

As per claim 2, Chen teaches, in view of above rejection, the CRC nullifier is one of a plurality of nullifiers (i.e., Figure 3A, reference numbers 336, 338 and 340), each having an output (i.e., Figure 3A, reference numbers 336, 338 and 340 have an output), and wherein the apparatus further comprises an output multiplexer (i.e., Figure 3A, reference number 342) coupled to the plurality of CRC nullifiers to select the output of one of the plurality of CRC nullifiers. The Examiner would like to point out that the output multiplexer is coupled to the nullifiers since, for example, the nullifier 338 is connected to control the output 372 and direct it to 310 which then relays it to the output multiplexer 342.

As per claim 3, Chen teaches, in view of above rejections, a data bus having N bytes (i.e., paragraph 0033, lines 2-4) coupled to the CRC calculator, wherein the plurality of CRC nullifiers comprise N-1 CRC nullifiers (i.e., Figure 3A, Y_0 to Y_{n-1} nullifiers).

As per claim 4, Chen teaches, in view of above rejections, a first multiplexer coupled to the CRC calculator (i.e., Figure 3A, reference number 326); and a second input multiplexer coupled to the CRC calculator (i.e., Figure 3A, reference number 332).

As per claim 5, Chen teaches, in view of above rejections, the first multiplexer (i.e., Figure 3A, reference number 326) is coupled to receive a data byte input signal (the input with reference number 370) and a feed zero signal (the input with reference number 362, which is the feed zero signal).

As per claim 6, Chen teaches, in view of above rejections, the second multiplexer (i.e., Figure 3A, reference number 332) is coupled to receive a default value input signal (input with reference number 387) and a CRC input signal (input with reference number 386).

As per claim 7, Chen teaches, in view of above rejections, the first multiplexer (i.e., Figure 3A, reference number 326) and the CRC calculator (i.e., Figure 3A, reference number 328) are each coupled to receive a byte enable signal (i.e., Figure 3A, reference number 352).

As per claim 8, Chen teaches, in view of above rejections, the CRC calculator performs a closed loop function (i.e., Figure 3A and paragraph 0059) and wherein the plurality of CRC nullifiers perform an operation outside of the closed loop function. The Examiner would like to point out that the nullifiers shown in Figure 3A (336, 338 and 340) operate outside of the closed loop function which only incorporates multiplexers 326, 328 and 324 (i.e., paragraph 0059).

As per claim 11, Chen teaches a method (i.e., paragraph 0002) comprising: receiving data on an input data bus having N byte width (i.e., Figure 3A and paragraph 0033), where N is greater than one (i.e., paragraph 0033, lines 5-7); and passing the data from the input data bus to a cycle redundancy check (CRC) computational circuitry having a CRC calculator (i.e., Figure 3A and paragraph 0033) and at least one nullifier (i.e., Figure 3A, reference numbers 336, 338 and 340 and paragraphs 0052-0055). The Examiner would like to explain the interpretation of the CRC nullifier. In paragraph 0011 (lines 9-12), Chen teaches to nullify a subset of the shift registers used in the CRC generator. Further in paragraphs 0052-0056, Chen performs the nullification process by programmable registers Y which are shown in Figure 3A and referred to by reference numbers 336, 338 and 340. Particularly, in paragraph 0055 (lines 5-9) Chen explains the nullifier by determining which of the coefficients take the value of 0.

As per claim 13, Chen teaches, in view of above rejections, performing a closed loop calculation function using the CRC calculator (i.e., Figure 3A, reference numbers 324, 326 and 328 and paragraph 0059); and performing a nullification function outside of the closed loop

calculation function using at least one nullifier (i.e., Figure 3A, reference number 338) of a plurality of nullifiers (i.e., Figure 3A, reference numbers 336, 338 and 340). The Examiner would like to point out that the nullification process is outside of the loop comprising of, for example, multiplexers 324, 326 and 328 (i.e., paragraph 0059).

As per claim 14, Chen teaches, in view of above rejections, to perform a closed loop calculation in a first cycle and the nullification is performed in one or more cycles following the first cycle (i.e., Figure 3A and paragraph 0031). The Examiner would like to point out that Chen teaches the ability to program and then reprogram, which means to calculate the CRC in a closed loop (i.e., paragraph 0059) and then reprogram by performing nullification (i.e., paragraphs 0052-0055) in a subsequent cycle.

As per claim 20, Chen teaches, an apparatus (i.e., Figure 3A and paragraph 0002) comprising: means for performing a closed loop calculation function using cycle redundancy check (CRC) calculator (i.e., Figure 3A, reference numbers 324, 326 and 328 and paragraph 0059); and means for performing a nullification function outside of the closed loop calculation function using a nullifier (i.e., Figure 3A, reference numbers 336, 338 and 340 and paragraphs 0052-0055). The Examiner would like to point out that the nullification process is outside of the loop comprising of, for example, multiplexers 324, 326 and 328 (i.e., paragraph 0059). Also, the Examiner would like to explain the interpretation of the CRC nullifier. In paragraph 0011 (lines 9-12), Chen teaches to nullify a subset of the shift registers used in the CRC generator. Further in paragraphs 0052-0056, Chen performs the nullification process by programmable registers Y which are shown in Figure 3A and referred to by reference numbers 336, 338 and 340.

Particularly, in paragraph 0055 (lines 5-9) Chen explains the nullifier by determining which of the coefficients take the value of 0.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 9, 10, 12, 15, 16, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (USPAN 2003/0093752A1) further in view of *Programmable Framer Chip Improves OC-48 Efficiency* by Louis E. Frenzel (herein after: Frenzel).

As per claim 9, Chen substantially teaches, in view of above rejections, a CRC calculator with nullification. See above rejection for claim 1.

Chen does not explicitly teach a framer with a link layer and physical interface as stated in the present application.

However, Frenzel teaches, in an analogous art, a programmable framer chip, which has the capability to dynamically allocate bandwidth in network communication (i.e., title). The Examiner would like to point out that the Physical layer/interface conveys the bit stream through the network at the electrical and mechanical level. It provides the hardware means of sending and receiving data on a carrier, including defining cables, cards and physical aspects. Fast Ethernet,

RS232, and ATM are protocols with physical layer components. Whereas at the link layer data packets are encoded and decoded into bits. The link layer furnishes transmission protocol knowledge and management and handles errors in the physical layer, flow control and frame synchronization. The data link layer is divided into two sub layers: The Media Access Control (MAC) layer and the Logical Link Control (LLC) layer. The MAC sub layer controls how a computer on the network gains access to the data and permission to transmit it. The LLC layer controls frame synchronization, flow control and error checking. Particularly, Frenzel teaches (page 2, paragraph 2) a WAN data link layer device or network processor through a POS-PHY bus. The Examiner would like to point out that the POS-PHY is analogous to the Physical interface and the WAN data link is analogous to the link layer. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the framer as taught by Frenzel with the CRC generator of Chen. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by using the framer with the CRC generator would have increased the efficiency of the system by dynamically allocating bandwidth (i.e., See Frenzel, page 1, paragraph 3 and page 3, paragraph 7).

As per claim 10, Frenzel substantially teaches, in view of above rejections, the physical interface is coupled to a first optical network (i.e., page 2, paragraph 3) and the link layer device is coupled to at least one of a second optical device and a copper network (i.e., page 2, paragraph 4).

As per claim 12, Chen substantially teaches, in view of above rejections, a method for CRC calculation with nullification. See above rejection for claim 11.

Chen does not explicitly teach receiving an end of packet character in the data and performing byte validation only when end of packet character is received as stated in the present application.

However, Frenzel teaches, in an analogous art, a programmable framer chip, which has the capability to dynamically allocate bandwidth in network communication (i.e., title). Particularly, Frenzel teaches (page 3, paragraph 2) another major benefit of the framer is that it can perform on-chip packet classification and tagging according to different bit fields. In other words, the framer taught by Frenzel teaches to detect the end of a packet and validating it. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the framer with end of packet verification as taught by Frenzel with the CRC generator of Chen. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by using the framer with end of packet verification with the CRC generator would have increased the efficiency of the system by increasing bandwidth for packet processing. (i.e., See Frenzel, page 3, paragraph 2).

As per claim 15, Chen substantially teaches, in view of above rejections, a method for CRC calculation with nullification. See above rejection for claims 11 and 13.

Chen does not explicitly teach performing an available transfer check and determining if a start of packet is available prior to performing closed looped calculation as stated in the present application.

However, Frenzel teaches, in an analogous art, a programmable framer chip, which has the capability to dynamically allocate bandwidth in network communication (i.e., title). Particularly, Frenzel teaches (page 3, paragraph 2) another major benefit of the framer is that it

can perform on-chip packet classification and tagging according to different bit fields. In other words, the framer taught by Frenzel teaches to detect the beginning of a packet. The Examiner would like to point out that a packet has to be received and made available prior to any calculation in the closed loop, which is the CRC calculation. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the framer with start of packet determination as taught by Frenzel with the CRC generator of Chen. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by using the framer with start of packet determination with the CRC generator would have increased the efficiency of the system by increasing bandwidth for packet processing. (i.e., See Frenzel, page 3, paragraph 2).

As per claim 16, Chen substantially teaches, in view of above rejections, determining if a byte valid value is equal to the input data bus width (i.e., Figure 4 and paragraph 0065); and appending zeros to an invalid data field if the byte valid is not equal to the input data bus (i.e., paragraph 0070). The Examiner would like to point out that Chen teaches (i.e., paragraphs 0065-0070) if the data input is not equal to the bus then the remaining inputs are set to zero which is essentially equivalent to stating that the remaining data fields are padded with zeros which is well known in the art.

As per claim 21, Chen substantially teaches, in view of above rejections, an apparatus for CRC calculation with nullification. See above rejection for claim 20.

Chen does not explicitly teach performing an available transfer check and determining if a start of packet is available prior to performing closed looped calculation as stated in the present application.

However, Frenzel teaches, in an analogous art, a programmable framer chip, which has the capability to dynamically allocate bandwidth in network communication (i.e., title). Particularly, Frenzel teaches (page 3, paragraph 2) another major benefit of the framer is that it can perform on-chip packet classification and tagging according to different bit fields. In other words, the framer taught by Frenzel teaches to detect the beginning of a packet. The Examiner would like to point out that a packet has to be received and made available prior to any calculation in the closed loop, which is the CRC calculation. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the framer with start of packet determination as taught by Frenzel with the CRC generator of Chen. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill would have recognized that by using the framer with start of packet determination with the CRC generator would have increased the efficiency of the system by increasing bandwidth for packet processing. (i.e., See Frenzel, page 3, paragraph 2).

As per claim 22, Chen substantially teaches, in view of above rejections, determining if a byte valid value is equal to the input data bus width (i.e., Figure 4 and paragraph 0065); and appending zeros to an invalid data field if the byte valid is not equal to the input data bus (i.e., paragraph 0070). The Examiner would like to point out that Chen teaches (i.e., paragraphs 0065-0070) if the data input is not equal to the bus then the remaining inputs are set to zero which is essentially equivalent to stating that the remaining data fields are padded with zeros which is well known in the art.

Allowable Subject Matter

Claims 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Also, Claim 17 would also need to terminate with a period as stated in the claim objections above.

Dependent claim 17 teaches, for example, performing the closed loop calculation function comprises: computing a CRC value over the input data bus width using the CRC calculator; determining if the current transfer does not contain a end of packet (EOP) character and, if so, feeding the calculated CRC value back as an old CRC value to the CRC calculator; and determining if the current transfer contains the EOP character. The prior arts of record do not teach, in singly or in combination, the forgoing limitations. Particularly, none of the prior arts of record teach or suggest, "...determining if the current transfer does not contain a end of packet (EOP) character and, if so, feeding the calculated CRC value back as an old CRC value to the CRC calculator; and determining if the current transfer contains the EOP character."

Dependent claims 18 and 19 further depend from dependent claim 17 and therefore are indicated as allowable subject matter as well.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts are included herein for Applicant's review. For example:

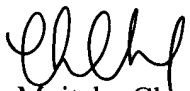
Gemelli et al. teach a method to generate the Cyclic Redundancy Check, or CRC, of data packets, minimizing computing time, particularly for the transmission of recursively embedded packets in packet-switching networks, particularly able to carry out the calculation even in case the packet length (as number of bits) is not a multiple integer of processed word width. The invention also concerns the CRC and checksum checking and computing machines carrying out the described calculation.

Poret et al. teach a single check field can be generated and appended to packets prior to a switching or other operation to support post-operation verification that protected fields were not altered during the operation and that the post-operation packet sequence matches the pre-operation packet sequence. The check field requires the use of nominally-synchronized packet counters at the check field generating system and at the verification system. The check field is generated by performing a CRC calculation on the protected fields of the packet. The CRC result is combined with the current packet count to obtain the final check field, which is appended to the packet. At the verification system, a CRC calculation is performed on the protected fields of the packet, included the appended final check field. This provides an interim check result which is compared to the current packet count at the verification system. A non-null compare result is indicative of an error condition. The type of error condition can be established by comparing verification results for successive packets.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mujtaba K. Chaudry whose telephone number is 571-272-3817. The examiner can normally be reached on Mon-Thur 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Mujtaba Chaudry
Art Unit 2133
January 11, 2007